CLAIMS:

What is claimed is:

1. A method of supporting memory addresses with holes, the method comprising the computer implemented steps of:

virtualizing a first physical address range allocated for system memory for an operating system run by a processor configured to support logical partitioning to produce a first logical address range;

virtualizing a second physical address range allocated for system memory for the operating system to produce a second logical address range, wherein the first physical address range and the second physical address range are non-contiguous and the first logical address range and the second logical address range are contiguous; and

virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective upper most logical address of the first and second logical address ranges.

2. The method of claim 1, wherein the steps of virtualizing the first physical address range, the second physical address range, and the memory mapped input/output physical address range comprises maintaining a mapping table that defines physical addresses and corresponding logical addresses.

3. The method of claim 2, wherein maintaining the mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges.

4. The method of claim 1, wherein the third logical address range is non-contiguous with the first logical address range and the second logical address range.

5. The method of claim 1, further comprising:

allocating a portion of at least one of the first physical address range and the second physical address range for a logical partitioning management software layer.

6. The method of claim 1, wherein the memory mapped input/output physical address range is allocated for cache inhibited addresses.

7. A computer program product in a computer readable medium for virtualizing non-contiguous physical memory ranges into a contiguous logical address range, the computer program product comprising:

first instructions for storing logical-to-physical memory address translations for first and second non-contiguous physical address ranges of a memory device

allocated for system memory and a third physical address range comprising a memory mapped input/output physical address range that is intermediate the first and second physical address ranges, and wherein a lower most logical address of the third physical address range provided by the logical-to-physical memory address translations is greater than an upper most logical address of first and second logical address ranges provided by the logical-to-physical memory address translations corresponding to the first and second non-contiguous physical address ranges; and

second instructions, responsive to execution of the first instructions, for converting a logical address into a corresponding physical address.

8. The computer program product of claim 7, wherein the logical-to-physical memory translations are stored in a mapping table that is unavailable to an operating system accessing the memory device.

9. The computer program product of claim 8, wherein the mapping table is maintained in at least one of the first and second physical address ranges.

10. The computer program product of claim 7, wherein the second instructions provide logical partitioning functionality.

11. The computer program product of claim 7, wherein the second instructions are maintained in at least one of the first and second physical address ranges.

12. The computer program product of claim 7, wherein the second instructions interface an operating system with input and output devices of a data processing system.

13. The computer program product of claim 12, wherein the second instructions present a contiguous logical address range comprising the first and second logical address ranges to the operating system.

14. The computer program product of claim 8, wherein the third physical address range is allocated for cache inhibited memory mapped input/output addresses.

15. A data processing system for supporting non-contiguous system memory arrays, comprising:

a memory that contains first and second non-contiguous physical memory arrays allocated for system memory having respective first and second physical address ranges and a third physical memory array having a third physical address range intermediate the first and second physical address ranges, a data set, and a set of instructions; and

a processor configured to support logical partitioning, wherein the processor, responsive to execution of the instructions, is presented with a

contiguous logical address range for accessing the first and second non-contiguous memory arrays.

16. The data processing system of claim 15, wherein the data set is a mapping table defining logical-to-physical memory address translations.

17. The data processing system of claim 15, wherein the set of instructions provides logical partitioning management.

18. The data processing system of claim 15, wherein the data set is maintained in the memory in at least one of the first and second physical address ranges.

19. The data processing system of claim 15, wherein the set of instructions are maintained in the memory in at least one of the first and second physical address ranges.

20. The data processing system of claim 15, wherein a second logical address range is mapped to the third physical address range, and a lower most logical address of the second logical address range is greater than an upper most logical address of the contiguous logical address range.